Larger wafers boosting GaAs and InP electronics

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The boom in the compound semiconductor industry was evident at both the GaAs MANTECH conference in Washington DC and the Indium Phosphide and Related Materials conference in Williamsburg, Virginia in May, with delegate and exhibitor numbers up by as much as 50% on last year. A key concern at both was supply of larger-diameter wafers — 6″ GaAs and 4″ InP — to meet demand for electronic devices.

According to GaAs MANTECH Program Chair Bruce A Bernhardt, demand for GaAs wafers is outstripping supply by 75% (driven by the trend to multi-mode, multi-band cell phones). Infineon's Otto Berger highlighted that the merchant GaAs market is forecast to increase from US$863m in 1998 (74% MESFET, 6% HEMT, 20% HBT) to US$2.9bn in 2003 (50% MESFET, 22% HEMT, 26% HBT). Meeting demand for the transition from 4″ to 6″ wafers is therefore critical.

Reports came from Motorola's Eugene Huang of the full conversion of its GaAs fab to 6″ by end-May, three months ahead of schedule (see Issue 4, page 4) and Filtronic on first samples at its new 6″ fab (see Issue 3, pages 38). In addition, several GaAs foundries are starting up using exclusively 6″ wafers, particularly in Taiwan (see Country Profile, this issue, page 42).

Global Communication Semiconductors (Torrance, CA, USA) is setting up a new fab in Hsinchu, Taiwan as Global Communication Technology Corp, expecting first 6″ HBT wafers out in May 2001. Though one of just a few "pure-play" GaAs foundries worldwide currently, several others are starting up in Taiwan.

One is WIN Semiconductors, a venture capital start-up formed in October '99 for GaAs HBT and pHEMT foundry in Hwaya Technology Park. WIN is due to begin volume production in March 2001 using only 6″ epi wafers (bought-in), ramping to 100,000 wafers per year by 2005. However, Donald P Mathes (vp of Production Planning & Expansion) is worried that "6″ demand will jerk the [supply] chain".

Demand for 6″ GaAs

The US government programmes MIMIC then TITLE III in the 1980s led to Litton Airtron, M/A-COM and American Xtal Technology delivering 6″ wafers in volume in the mid-'90s. However, it wasn't until 1998 that the first 6″ GaAs fab was opened by Vitesse (followed in 1999 by Anadigics, then Motorola and Infineon). Otherwise, said Thomas Anderson (Litton's Chief Technology Officer and vp of Business Development in a "GaAs roadmap" panel discussion) "6″ could have been here five years ago".

Fearing that the market wouldn't develop, many suppliers have been cautious about investing in 6″, especially in Japan where demand for microelectronics is less, with some having just one 6″ crystal puller and turning more to epi (entirely, in the case of Japan Energy). Dowa Mining's Yuji Matsusaka says it started test operation of its 6″ plant in June '99 but was "hesitating to invest in capacity because of its bad experience on the transition from 3″ to 4″". Hitachi Cable only started production in its Fab 2 in August '99 but in February said it was spending a further ¥7.2bn on plant and equipment to increase capacity this year from 20,000 to 30,000 wafers per month (70% 4″: 30% 6″).

Freiberger Compound Materials' 6″ capacity is 50,000 wpy (already exceeding their 100,000 4″ wpy capacity by area), compared to a demand of 70,000 wpy, says managing director Dr Tilo Flade. Despite output this year expected to be 80% up on 1999, they are still booked up till May 2001 for both 6″ and 4″ wafers, when Fab II will start up.

A major bottleneck is that 6″ LEC crystal pullers are taking 6-12 months to bring on-line, says M/A-COM's Technical Applications Manager III-V Materials Judy Kronwasser. One possible consequence is that the shortage of GaAs could force chip companies to turn to SiGe, while Picogiga also warns that if they don't get the price of 6″ epi wafers down to US$800 then business could return to implantation (i.e. MESFETs).

By contrast, AXT makes 6″ GaAs by VGF, which uses low-pressure reactors that are quick to self-assemble and change diameter. AXT was installing four new reactors a week and plans to triple 6″ capacity by end-Q3/2001 from this May's 5000 wafers per month. AXT also claims an order of magnitude

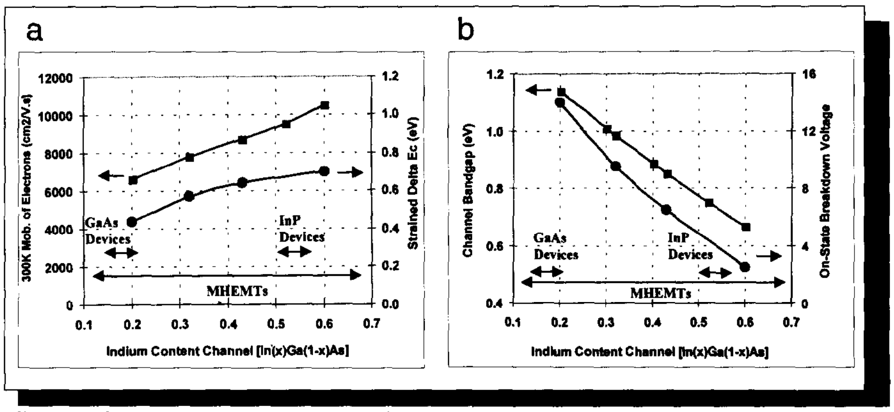

Figure 1. Adding indium to the channel (a) increases both the mobility and well depth (for a strained InAlAs barrier layer) and (b) reduces both bandgap and on-state breakdown voltage. (Courtesy of C S Whelan, Raytheon RF Components)

fewer defects than LEC growth.

Freiberger has also made 4″ wafers by VGF since 1999 and developed 6″ VGF this year (for production by end-2000). Dowa is now also making wafers by VGF, although capacity is currently taken up by demand for semiconducting GaAs for lasers rather than semi-insulating GaAs.

Demands of 6″ on process technology

Another implication of 6″ wafers arose in a session on "Etch". PlasmaTherm, Motorola and the University of Florida addressed how, compared to the 10-30 mTorr of conventional production Reactive Ion Etching, the lower pressure of 2 MHz-based Inductively Coupled Plasma etching (2-10 mTorr) can achieve higher across-wafer uniformity (critical for 6″ wafers) of <±5% on an electrostatic chuck for high-selectivity etching (>50-100:1) of GaAs over $Al_xGa_{1-x}As$ (for x>0.1), as well as over InGaP and InGaAs (see article on Etch, page 48).

Metamorphic-HEMTs vs lattice-matched InP

Larger wafers are also giving added impetus to InGaAs-channel devices with higher indium content than is possible in pseudomorphic HEMTs. This can be done by growing metamorphically on GaAs (via lattice-constant-shifting graded-composition buffer layers) rather than lattice-matched on 2-3" InP.

In the $In_xGa_{1-x}As$ channel of HEMTs, increased indium composition x lowers the effective mass of electrons, increasing mobility (see Figure 1a) and therefore device speed. A GaAs substrate allows pseudomorphic growth (on an AlGaAs buffer layer) but limited to about x <0.22. The larger lattice parameter of InP allows growth either lattice-matched (LM) for $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ or pseudomorphically on an InAlAs buffer for x=0.3-0.65 (limited by the lowering of breakdown voltage). This enables cut-off frequencies up to 300 GHz at 0.1 μm gate length, giving a performance advantage for sub-100 GHz applications (e.g. for millimetre-wave Local Area Networks, radio links up to 55 GHz, 77 GHz car radar, and 40 Gb/s optical communications). Also, a higher conduction band offset with the barrier layer (Figure 1a) gives greater carrier confinement in the channel. This results in higher gain-bandwidth and lower noise figure at higher frequencies than any other type of transistor.

However, InP has higher substrate cost (US$50 vs to US$15 per sq.-in) and processing cost (with greater fragility and lower yield), immature back-side etching and wafer thinning processes, as well as smaller-diameter wafers (2″ and 3″). By comparison, added the speaker from Sanders, GaAs pHEMT process technology is more mature, higher yield and currently half the cost. However, power performance is marginal and about 10% lower in efficiency and 2 dB lower in power gain at 60 GHz.

Interest is therefore being shown in using a metamorphic buffer layer of linear - or step-graded composition (and therefore lattice constant) to relax the strain of the 4% lattice mismatch between a GaAs substrate and an x=0.3-0.65 $In_xGa_{1-x}As$ channel, trapping misfit dislocations before they reach the active layer. This combines InP-type device performance with GaAs costs for processing.

Unfortunately, raising In content reduces the channel's bandgap energy and breakdown voltage (see Figure 1b). However, the lattice-constant-shifting allows a wider range of Al and In compositions in the buffer, enabling the engineering of an active-layer heterostructure with larger conduction band discontinuity (e.g. $In_{0.65}Ga_{0.35}As/In_{0.4}Al_{0.6}As$). This gives better quantum-well confinement and less parallel conduction as well as improved off-state breakdown.

But, to achieve this, metamorphic buffers need to be smooth and strain compensated.

Sb- versus As- and P-based buffers

Sanders reported on 0.1 μm power MHEMTs on 3″ GaAs using a 1 μm thick AlGaAsSb strain-relieving buffer layer, providing a smoother surface for MMIC processing than As- or P-based buffers and allowing a 65% In channel (compared to 32-50% for other GaAs-based power MHEMTs). Despite using a mask designed for InP HEMTs, record power MHEMT MMIC performance was achieved: at 60 GHz output power was 185 mW, power gain 6.9 dB and Power Added Efficiency 41.2% (comparable to Sanders' best InP HEMT MMICs).

D Lubyshev of QED (with Raytheon, Sanders, the Army Research Lab and E.P.I.) compared $In_{0.53}Ga_{0.47}As$-channel MHEMTs grown by MBE on As-based InAl(Ga)As, P-based InAlP and Sb-based AlGaAsSb graded-composition buffers.

For InAlGaAs buffers, starting the grading at 25%Ga and 75%Al and growing at 400°C yielded an extremely rough surface. However, this was alleviated by starting at 12%Ga and grading the In%, Ga% and Al% simultaneously, as well as growing at 350°C and reducing the V/III ratio slightly. Grading In from 3% to 53% showed better surface morphology, but grading from 3% to a 63% overshoot followed by an inverse-graded strain relaxation step back to 53% showed higher mobility. Channel charge density was up 29% (compared to a reference LM-HEMT) and roughness was 13.9Å (for a 1.1 μm-thick buffer).

InAlP linearly graded from 47%In (lattice matched on GaAs) to 100% was comparable to LM-HEMTs in electrical transport properties and surface morphology (with roughness of 60Å) but not as good as the As-based MHEMTs. Channel charge density was up 10%.

AlGaAsSb buffers with step-graded Sb concentrations (for complete strain relaxation) had mobilities comparable to LM-HEMTs and roughness 13Å. However, "the complicated grading procedure and potential cross contamination may hinder the transfer of Sb-based MHEMT technology to multi-wafer MBE reactors for volume production".

Hitachi Cable's speaker agreed that antimonide buffers achieve superior surface flatness, but there is reluctance to adopt Sb due to "difficulties in the chemical etching process". IMEC's speaker added that, due to the "complexity of growth of quaternary material by MBE, ternary materials are most commonly used".

P C Chao and K Nichols of Sanders acknowledge that AlInAs buffers are "more compatible with conventional [pHEMT] MBE systems", but only because they already have Ga, Al, In, and As sources. However, QED grew Sb buffers at the end of a cycle before a planned shut-down and clean, Amy Liu indicating that the system came back on-line without showing any ill effects from antimony. Chao argues that better surface morphology actually makes Sb-based MHEMTs easier to process.

The best results reported by both Raytheon and QED use a III-arsenide quaternary, AlInGaAs (rather than a III-III-V-V). Both claim improvements in reproducibility and device results by lowering the Ga flux while raising the In flux (ramped in opposite directions to keep the growth rate constant). However, Chao and Nichols argue that, since there are currently no valved group III sources, AlInAs and AlInGaAs buffers require the In (or the In and Ga together) to be thermally ramped to change the flux. This necessitates a compromise: if the large cells of a production MBE machine are used and are fully loaded with material then the thermal ramp rate extends the buffer growth time, lowering throughput and raising cost; if partially loaded to increase thermal ramp rate, then system uptime is reduced (doubly costly for AlInGaAs, as well as requiring synchronisation of Ga and In renewal).

In contrast, while the antimonide buffer is a quaternary (AlGaAsSb), the ratio of Al to Ga is constant throughout the buffer-layer grading process - also, the exact ratio is not critical compared to the As and Sb fluxes (for which valved sources are available) so buffer growth is not limited by thermal ramp rates.

The first MHEMTs on 4″ GaAs (rather than 3″) has been demonstrated by TriQuint, using a production foundry to allow faster technology transfer (with engineering supervision on just a few steps such as gate recessing). Buffers were $Al_xIn_{1-x}As$ (x=0.40-0.53) and gate length 0.15 μm. A composite channel of $In_{0.63}Ga_{0.37}As$ and $In_{0.53}Ga_{0.47}As$ yielded an extrapolated f_T of 150 GHz (compared to 80 GHz for pHEMTs). An $In_{0.43}Ga_{0.57}As$ channel gave frequency performance comparable to InP LM-HEMTs: a record MHEMT noise figure at 26 GHz of 0.73 dB (0.3 dB less than same-gate-length pHEMTs) and an associated gain of 12.6 dB (2-3 dB higher). Mobility was >10,000 cm^2/Vs (50% up on pHEMTs).

The first growth of MHEMTs by MOCVD ("indispensable for commercialisation") was reported by T Tanaka of Hitachi Cable's Advanced Research Centre. This included the use of phosphorous-containing GaInP and InP for an etch-stop (to increase yield) and a surface passivation layer (to increase breakdown voltage). The buffer was step-graded from $In_{0.15}Al_{0.85}As$ to $In_{0.35}Al_{0.65}As$ (with the wide bandgap giving resistivity of 10^8 Ω cm). The $In_{0.36}Ga_{0.64}As$ channel had mobility of 8,300 cm^2/Vs (comparable with MBE) perhaps due to interface roughness of no more than 5 nm in a period of 1 μm despite the 2.6% lattice mismatch. MBE structures grown for comparison (at the low temperature of 350-450°C needed for high electron mobility) showed more frequent roughness than MOCVD growth (at >550°C).

4″ InP wafers at IPRM

A topic of controversy at GaAs MANTECH - but not at IPRM - was the availability of 4″ InP wafers.

The main driver is not opto but the larger die size of microelectronic devices. Previously applications have mainly been military. While there are nine suppliers of 3″ InP wafers, there

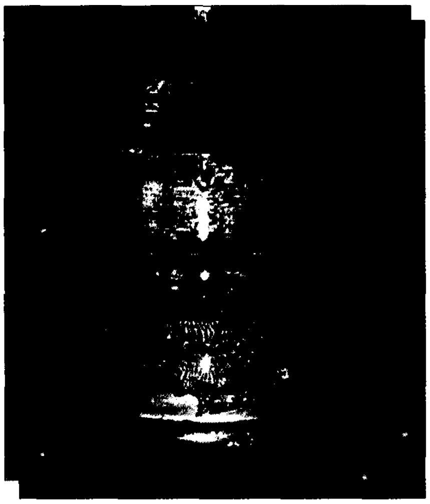

Figure 2. M/A-COM's 4″ InP crystals, grown in a standard CI358 (now MR358) puller.

are just four supplying 4″ semi-insulating wafers: AXT and M/A-COM (both funded by the US defence Title III programme from 1997 to April '99), Crystacomm, and Sumitomo. Commercial applications are growing, but concerns are material quality and manufacturability.

Some point out the variation in diameter along a 4″ InP boule. But M/A-COM's Rowland Ware says that all boules are grown over wafer diameter (by about 10 mm - see Figure 2) then ground to size, so this is not significant. The 4″ wafers tend to have a higher dislocation density than 3″ but this is also "not a significant factor at present". "Probably the company most committed to 4″ InP is Nortel" (whose Carla Miner gave a presentation on characterisation), while Vitesse "certainly seem to be serious [about 4″ InP]" and will initially employ a foundry. "Another company making noises is Anadigics".

InP HEMTs and HBTs

NTT Photonic Labs' director Horoshi Yoshimura in his plenary talk explained how GaAs is sufficient for 10Gb/s data-rate fibre-optic transmission, but by 2004 40Gb/s data rates will require f_T = 200 GHz, necessitating a 0.1 µm-gate InP heterojunction FETs (using hybrid e-beam and optical lithography) - compatible with NTT's 3″ GaAs processes.

TRW's HBT section manager A Gutierrez-Aitken said they are delivering over 4m GaAs HBTs and HEMTs per month and are now - after 10 years of developing InP HBT and HEMTs for space and defence applications - adapting multi-wafer MBE technology for the first commercial 40 Gb/s InP products, with line yield >90% (comparable to GaAs).

However, previously the low breakdown voltage of a high-In InGaAs channel has limited high power applications, but to improve power and efficiency TRW is taking two approaches:

- Use an InGaAs/InP composite channel. At low drain-to-source voltage electrons are confined in the high-mobility, high-saturation-velocity InGaAs layer; at high voltage some are transferred into the InP layer, where the avalanche breakdown threshold is much higher. This enables higher drain bias voltage without compromising RF performance at higher frequencies.
- Increase Al composition in the Schottky barrier layer as well as In composition in the channel to 75%.

TRW reported operation of a 0.15 µm-gate InP HEMT MMIC at 21 GHz with output power and PAE comparable to a 0.15 µm GaAs HEMT but with higher associated gain and lower drain voltage.

Fujitsu reported MOCVD-grown 50 nm-gate LM-HEMTs with f_T = 362 GHz, a record for any transistor. This is thought to be due to the difference between the actual gate metal length and the effective gate length (through side etching of the gate recess and expansion of the carrier depletion region with high drain-to-gate voltage) being much shorter (16 nm) than for the previous bests of 340 GHz for a 50 nm-gate $In_{0.8}Ga_{0.2}As$-channel InP pHEMT and 350 GHz for a 30 nm-gate InP LM-HEMT. This is possibly due to the low temperature, <300°C, preventing fluorine contamination and suppressing diffusion of the Si-delta-doped sheet and degradation of the epi structure.

HRL Labs and Jet Propulsion reported MBE-grown 0.1 µm gate pHEMT MMICs with a $In_{0.8}Ga_{0.2}As$/InP composite channel (Si-doped on both sides) and $In_{0.52}Al_{0.48}As$ buffer. Electron density was 4×10^{12} cm^{-2} and mobility >10,000 cm^2/Vs), yielding f_T > 250 GHz and f_{max} > 600 GHz.

HRL also reported a next-generation high-power, high-frequency InP HEMT. Despite a lower-In $In_{0.6}Ga_{0.4}As$ channel, the use of a composite buffer layer with $In_{0.52}Al_{0.48}As$ and a wider-bandgap (1.9 eV) $In_{0.36}Al_{0.64}As_{0.84}Sb_{0.16}$ Schottky layer creates a larger channel conduction-band discontinuity and higher Schottky barrier at the gate. This gives 20% higher current density, 10% higher transconductance and higher breakdown voltage. Short-channel effects (e.g. weak pinch-off, high output conductance) are alleviated, allowing a shorter gate length (0.08 µm) for higher f_T without degrading f_{max}. Preliminary data predicts both over 300 GHz.

Recently, InP HEMT MMIC power amps with e-beam-written gate fingers have shown higher gain than HBTs and have dominated W-band applications. However, Nortel Networks and University of California Santa Barbara reported InGaAs/InAlAs/InP HBT MMIC amps with record power performance at W band: 11.7 mW (10.7 dBm) at 78 GHz under 1 dB of gain compression. This was achieved by scaling the emitter and collector junction widths and reducing extrinsic device parasitic capacitance by substrate transfer to access both sides of the epitaxial film. Introduction of InP collectors are expected to increase breakdown voltage and hence output power.

MM-HBTs

Compared to MHEMTs, there have not been many reports of metamorphic HBTs, since HBTs are minority-carrier devices. However, Singapore's Nanyang Technological University has reported the first self-aligned InP/InGaAs metamorphic double-heterojunction bipolar transistors (MM-DHBTs) grown by Solid-Source MBE on GaAs substrates (also the first Al-free MHEMT).

A composite collector $In_{0.53}Ga_{0.47}As/InP$ (to avoid current blocking) was grown by MBE on 2″ GaAs using a linearly-graded 1.5 μm InGaP buffer layer (In=0.48-1, finding an optimum growth temperature of 480°C) for 96% strain relaxation. f_T = 46 GHz and f_{max} = 40 GHz were achieved. Compared to InP LM-HBTs, the lower f_{max} is due to the degradation of f_T as a result of increased base and collector transit times. This is due to degradation of base-emitter interface quality (observed as rough surface morphology, and causing either a lower energy band discontinuity or non-abrupt junction) and the increase of bulk recombination. Optimisation of the buffer-layer growth conditions or use of other buffer layers (e.g. Sb-containing strain relief buffer, which tends to give a smoother surface) could improve DC and RF performance.

In fact, the first GSMBE-grown InP/GaAsSb/InP DHBTs were also reported, grown at Agilent Labs and processed at Simon Fraser University. The staggered band line-up of $InP\text{-}GaAs_{0.51}Sb_{0.49}$ heterojunctions (ΔE_v=0.78 eV; ΔE_c= -0.15 eV) allows non-blocking abrupt-junction DHBTs with simpler device design and implementation than InGaAs-based DHBTs. For a 400Å $GaAs_{0.51}Sb_{0.49}$ base and a 3000Å InP collector, compared to f_T = 80 GHz for MOCVD, f_T was a record 110 GHz and f_{max} = 62 GHz, due to the base transit time possibly from improved minority carrier mobility.

The Michael Lunn Memorial Award was presented at IPRM '00 to Professor Shigehisa Arai of the Tokyo Institute of Technology for "initial demonstration of 1.55 μm GaInAsP/InP CW lasers and continuing contributions to InP-based advanced semiconductor lasers".